

1 CLAIM LISTING

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3 1. (Currently amended) A substrate with a via and pad structure for
4 connecting a component to conductive layers of the substrate, comprising:
5 a substrate;
6 a plated via connected to the conductive layers;
7 a solder mask surrounding the plated via; and
8 a conductive pad with a conductive trace connected to the plated via, wherein the
9 solder mask exposes a part of the conductive pad that extends beyond the terminal
10 sides of the component to increase solder formation at the terminal sides.

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12 2. (Original) The substrate with the via and pad structure of claim 1, wherein
13 the solder mask reduces solder formation at the terminal end of the component.

14
15 3. (Original) The substrate with the via and pad structure of claim 2, wherein
16 the conductive pad includes a first arm and a second arm that extend beyond the
17 terminal sides of the component.

18
19 4. (Original) The substrate with the via and pad structure of claim 3, wherein
20 the first arm and the second arm are symmetrically disposed on the substrate with
21 respect to the plated via.

22
23 5. (Original) The substrate with the via and pad structure of claim 2, wherein
24 the conductive pad includes a first arm, a second arm, and a body.

25
26 6. (Original) The substrate with the via and pad structure of claim 5, wherein
27 the first arm and the second arm are symmetrically disposed on the substrate with
28 respect to the plated via.

29
30 7. (Original) The substrate with the via and pad structure of claim 2, wherein
the conductive pad includes a T-shirt shaped structure.

1 8. (Original) The substrate with the via and pad structure of claim 7, wherein
2 the T-shirt shaped structure is symmetrically disposed on the substrate with respect to
3 the plated via.

4
5 9. (Original) The substrate with the via and pad structure of claim 2, wherein
6 the solder mask is keyhole shaped.

7
8 10. (Original) The substrate with the via and pad structure of claim 2, wherein
9 the solder mask covers the substrate partially or entirely except the conductive pad and
10 the plated via.

11
12 11. (Original) The substrate with the via and pad structure of claim 2, further
13 comprising a component electrically connected to the conductive pad through solder
14 joint(s), wherein the solder joints have a greater volume at the terminal sides than at the
15 terminal end of the component.

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17 12. (Original) The substrate with the via and pad structure of claim 2, wherein
18 the substrate is part of a printed circuit board.

19
20 13. (Original) The substrate with the via and pad structure of claim 2, wherein
21 the substrate is part of a BGA package.

22
23 14. (Currently amended) A substrate with a plurality of via and pad structures
24 for connecting a component to conductive layers of the substrate, comprising:

25 a substrate;

26 a first plated via connected to the conductive layers;

27 a first solder mask surrounding the first plated via;

28 a second plated via connected to an associated conductive layer;

29 a second solder mask surrounding the second plated via;

30 a first conductive pad with a conductive trace connected to the first plated via,

wherein the first conductive pad includes a portion that is exposed to solder and

1 extends beyond the terminal sides of the component to increase solder formation along
2 the terminal sides; and

3 a second conductive pad with a conductive trace connected to the second plated
4 via, wherein the second conductive pad includes a portion that is exposed to solder and
5 extends beyond the terminal sides of the component to increase solder formation along
6 the terminal sides.

7
8 15. (Original) The substrate with the plurality of via and pad structures of
9 claim 14, wherein the first solder mask reduces solder formation at one terminal end of
10 the component and the second solder mask reduces solder formation at the other
11 terminal end of the component.

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13 16. (Currently amended) The substrate with the plurality of via and pad
14 structures of claim 15, wherein each of the first and second conductive pads include a
15 first arm[,] and a second arm.

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17 17. (Original) The substrate with the plurality of via and pad structures of
18 claim 16, wherein each of the first and second conductive pads is symmetric to the first
19 plated via and the second plated vias, respectively.

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21 18. (Original) The substrate with the plurality of via and pad structures of
22 claim 15, wherein the first and second conductive pads include a first arm, a second
23 arm, and a body.

24
25 19. (Original) The substrate with the plurality of via and pad structures of
26 claim 18, wherein each of the first and second conductive pads is symmetric to the first
27 plated via and the second plated vias, respectively.

28
29 20. (Original) The substrate with the plurality of via and pad structures of
30 claim 15, wherein each of the first and second conductive pads include a T-shirt shaped
structure.

1 21. (Original) The substrate with the plurality of via and pad structures of
2 claim 20, wherein each of the T-shirt shaped structures is symmetric to the first and
3 second plated vias, respectively.
4

5 22. (Original) The substrate with the plurality of via and pad structures of
6 claim 15, wherein each of the first and second solder masks is a ring surrounding the
7 first and second plated vias, respectively.
8

9 23. (Original) The substrate with the plurality of via and pad structures of
10 claim 15, wherein each of the first and second solder masks is a keyhole shape and
11 surrounds the first and second plated vias, respectively.
12

13 24. (Original) The substrate with the plurality of via and pad structures of
14 claim 15, wherein each of the first and second solder masks cover the substrate
15 partially or entirely except the first and second conductive pads and the first and second
16 plated vias.
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18 25. (Original) The substrate with the plurality of via and pad structures of
19 claim 15, further comprising a component electrically connected to the first and second
20 conductive pads through solder joint(s), wherein the solder joint(s) have a greater
21 volume at each of the terminal sides than at each terminal end of the component.
22

23 26. (Original) The substrate with the plurality of via and pad structures of
24 claim 15, wherein the separation along the substrate between the first and second
25 solder masks defines the length of the component to be soldered.
26

27 27. (Original) The substrate with the plurality of via and pad structures of
28 claim 15, wherein the substrate is part of a printed circuit board.
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30 28. (Original) The substrate with the plurality of via and pad structures of
claim 15, wherein the substrate is part of a BGA package.

1 29. (Original) The substrate with the via and pad structure of claim 2, wherein
2 solder mask is a ring surrounding the plated via.

3
4 30. (Withdrawn) A method of reducing solder wicking on a substrate with
5 associated conductive layers, comprising:

6 (a) forming a via and pad structure;

7 (b) masking around the plated via to reduce solder formation at the plated via;

8 (c) placing a component having terminal sides and a terminal end on the
9 conductive pad;

10 (d) extending the conductive pad beyond the terminal sides of the component to
11 increase solder formation along the terminal sides; and

12 (e) soldering the component to the conductive pad.

13
14 31. (Withdrawn) The method of claim 30, further comprising repeating steps
15 (a) through (e) for a plurality of via and pad structures.

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17 32. (Withdrawn) The method of claim 30, wherein the conductive pad is a T-
18 shirt shaped structure.

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20 33. (Withdrawn) The method of claim 31, wherein the masking around plated
21 via is accomplished by a keyhole shaped structure.

22
23 34. (Withdrawn) The substrate with the plurality of via and pad structures of
24 claim 14, wherein the first conductive pad extends beyond the terminal side of the
25 component a maximum distance that reduces solder wicking without generating
26 electrical shorts between the first conductive pad and an adjacent plated via.

27
28 35. (Withdrawn) A computer implemented method for calculating the
29 maximum distance of a conductive pad extending beyond the terminal side of a
30 component, wherein the component is placed diagonally in an array of four plated vias,
comprising:

1 (a) storing L1 representing the center-to-center distance of a first plated via and a
2 second plated via;

3 (b) storing L3 representing the length and L4 the width of the component;

4 (c) storing L5 representing the length of the conductive pad extending beyond the
5 terminal side;

6 (d) storing R representing an outer radius of a first plated via;

7 (e) storing X representing the minimum distance between the first plated via and
8 the conductive pad;

9 (f) calculating L2, representing the center-to-center distance between the first
10 plated via and a third plated via, by dividing L1 by $\sin 45^\circ$;

11 (g) calculating L8, representing the distance from the center of the first plated via
12 to the side of the component, by subtracting L4 from L2 and dividing by two;

13 (h) calculating L7, representing half the distance between the conductive pad and
14 an opposite conductive pad, by dividing L3 by two and subtracting L5;

15 (i) calculating L11 by summing R and X;

16 (j) calculating L9 by taking the square root of the difference of the square of L11
17 and the square of L7; and

18 (k) calculating L10 by subtracting L9 from L8, wherein L10 is the maximum
19 distance of the conductive pad extending beyond the terminal side of the component.
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